



FIG. 4

ROM CELL TRANSISTOR SUBTHRESHOLD LEAKAGE CURRENT
(N-CHANNEL, $V_d = 1.32\text{v}$)

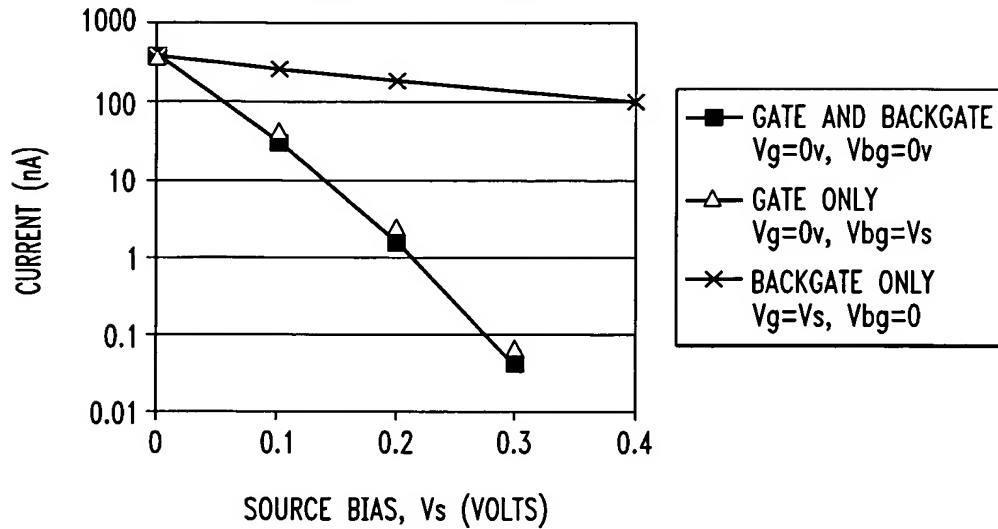


FIG. 5

ROM CELL TRANSISTOR SATURATION CURRENT
(N-CHANNEL, $V_d = 1.08\text{v}$)

